REMARKS/ARGUMENTS

Claims 1, 8-10 and 12-14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chau in view of Tsai; claims 2-7 and 11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai as applied to claims 1 and 8-10, and further in view of Wolf.

The Chau patent does not disclose and method for forming the interconnect structure and such a description must necessarily come from the Tsai patent. The Tsai patent discloses forming a silicon oxide layer 13 adjacent the gate electrode 12 (col. 4, lines 53-55). A titanium nitride layer sidewall spacer 14 is formed adjacent the silicon oxide layer 13. The Tsai et al. patent teaches "[I]n this invention the risk of bridging is eliminated via the removal of the top layer of the dual insulator spacer titanium nitride 14 during the unreacted titanium removal procedure" (col. 5, lines 53-56). The Tsai et al. patent teaches the removal of the titanium nitride layer 14. Figure 8 of the Tsai et al. patent shows the complete removal of the titanium nitride layer. There is no material left after etching and there is no inherency as suggested by the examiner. In fact the choice of titanium nitride for use in forming the spacer layer 14 was predicated on not leaving any material after the removal process. The layer 28 described by the examiner as the pre-metal spacer layer is formed adjacent the silicon oxide layer 13 as shown in Figure 13. There is no nitride layer remaining as it has been completely removed as described above. This limitation of claim 1 of the instant invention is not found in either patent cited by the examiner and claim 1 is therefore allowable over the cited art. Claims 8-10 and 12 – 14 all depend from claim 1 and contain the limitations of claim 1. Claims 8 – 10 and 12 – 14 are therefore also allowable over the cited art.

Claims 2-7, and 11 all depend from claim 1 and contain the limitations of claim 1. As described above claim 1 is allowable over the Tsai et al. patent. The Wolf reference does not contain the limitation of etching the nitride spacer layer and so cannot be properly combined with the Tsai et al. patent under 35 U.S.C. 103(a) to reject claims 2-7, and 11-14. Claims 2-7, and 11-14 are therefore allowable over the cited art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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